

WHAT IS CLAIMED IS:

- 1 1. An SRAM memory cell comprising:
2 first and second inverters interconnected between first and second data nodes,
3 each inverter comprising complementary MOS transistors connected in series between a DC
4 voltage reference and a ground reference, and
5 means for programming the MOS transistors adapted for causing, after
6 programming, an irreversible degradation of a gate oxide layer of some at least of the transistors.
- 1 2. The SRAM memory cell according to Claim 1, wherein each inverter comprises a
2 first PMOS transistor and a second NMOS transistor coupled in series between the voltage
3 reference and the ground reference, the data nodes (N1, N2) being formed respectively between
4 the two NMOS and PMOS transistors of the inverters.
- 1 3. The SRAM memory cell according to Claim 1 wherein the degradable MOS
2 transistor is a thin gate oxide layer transistor.
- 1 4. The SRAM memory cell according to Claim 3, wherein the oxide layer is
2 degradable at least locally in such a way as to obtain, during the reading of the cell, a variation in
3 the current delivered by the transistor.

1 5. The SRAM memory cell according to Claim 1, wherein the programming means
2 comprise, for each inverter, a programming transistor (28, 30) or a diode linked between a
3 programming control line (PROG) and one of the transistors of the inverter.

1 6. The SRAM memory cell according to Claim 5, wherein the programming means
2 comprise one of an NMOS transistor or a programming diode that selectively links the gate of
3 the degradable transistor to a programming voltage reference delivering a voltage level able to
4 cause, jointly with the DC voltage supply source linked to the drain of the degradable transistor,
5 a degradation in the gate oxide layer of the transistor, the programming transistor being driven by
6 the programming control line.

1 7. The SRAM memory cell according to Claim 1, further comprising means for
2 causing the cell to operate as an SRAM memory after programming.

1 8. The SRAM memory cell according to Claim 7, wherein the inverters are
2 interconnected by way of NMOS transistors linked to a control line for instructing the cell to
3 operate as an SRAM memory.

1 9. The SRAM memory cell according to Claim 8, wherein a drain electrode and
2 source electrode of each of the said NMOS transistors are respectively linked to the gate of the
3 transistors of one of the inverters.

1 10. An SRAM memory cell of the 6T type which includes a pair of load transistors
2 connected to a reference voltage, the memory cell further including a programming circuit
3 coupled to a gate of at least one of the load transistors, the programming circuit delivering a
4 voltage to the gate of the at least one load transistor which is sufficient to cause an irreversible
5 gate oxide degradation for purposes of programming the memory cell to permanently store a
6 certain data value.

1 11. The SRAM memory cell of claim 10 wherein the programming circuit comprises
2 a programming transistor having a source/drain terminal connected to a gate of the at least one
3 load transistor and a drain source terminal connected to a voltage reference.

1 12. The SRAM memory cell of claim 10 wherein the programming circuit comprises:
2 a first programming transistor having a source/drain terminal connected to a gate
3 of a first one of the load transistors and a source/drain terminal connected to a voltage reference;
4 and
5 a second programming transistor having a drain/source terminal connected to a
6 gate of a second one of the load transistors and a source/drain terminal connected to the voltage
7 reference.

1 13. The SRAM memory cell of claim 12 wherein the first and second programming
2 transistors are connected in series with each other.

1 14. An SRAM memory cell of the 6T type including a pair of inverter transistors
2 which are cross-coupled and a pair of load transistors, the memory cell further including a
3 operational configuration circuit that selectively connects and disconnects a gate of a first load
4 transistor to a gate of a first inverter transistor and selectively connects and disconnects a gate of
5 a second load transistor to a gate of a second inverter transistor.

1 15. The SRAM memory cell of claim 14 wherein operational configuration circuit
2 comprises a pair of control transistors whose gates are connected to receive a control signal, a
3 first control transistor having its source terminal connected to a gate terminal of a first load
4 transistor and its drain terminal connected to a gate terminal of a first inverter transistor, and a
5 second control transistor having its drain terminal connected to a gate terminal of a second load
6 transistor and its source terminal connected to a gate terminal of a second inverter transistor.

1 16. The SRAM memory cell of claim 14, further comprising a programming circuit
2 coupled to the gate of at least one of the load transistors, the programming circuit delivering a
3 voltage to the gate of the at least one load transistor which is sufficient to cause an irreversible
4 gate oxide degradation for purposes of programming the memory cell to permanently store a
5 certain data value.

1 17. The SRAM memory cell of claim 16 wherein the programming circuit comprises
2 a programming transistor having a source/drain terminal connected to a gate of the at least one
3 load transistor and a drain source terminal connected to a voltage reference.

1 18. The SRAM memory cell of claim 10 wherein the programming circuit comprises:
2 a first programming transistor having a source/drain terminal connected to a gate
3 of a first one of the load transistors and a source/drain terminal connected to a voltage reference;
4 and
5 a second programming transistor having a drain/source terminal connected to a
6 gate of a second one of the load transistors and a source/drain terminal connected to the voltage
7 reference.

1 19. A method for operating an SRAM memory cell of the 6T type, comprising:
2 delivering a voltage to a gate of at least one load transistor in the SRAM memory
3 cells which is sufficient to cause an irreversible gate oxide degradation for purposes of
4 programming the memory cell to permanently store a certain data value.

1 20. The method of claim 19 further comprising selectively connecting and
2 disconnecting the gate of each load transistor to a gate of its series connected inverter transistor
3 in the SRAM memory cell.